CLAIMS

What is claimed is:

1. A current-controlling device comprising:

a first conductor and a second conductor;

a tunneling barrier comprising a first insulation layer, the tunneling barrier electrically isolates the first conductor from the second conductor;

at least one mobile charge positionable within the tunneling barrier; and

a gate, wherein a voltage applied to the gate moves the mobile charge to a position between the first conductor and the second conductor within the tunneling barrier, thus deforming the shape of the energy barrier between the first conductor and the second conductor.

2. The device of claim 1, wherein the first conductor and the second conductor are formed on a substrate, further comprising a second insulating layer positioned between the substrate and: the first conductor; the second conductor; and the tunneling barrier.

3. The device of claim 2, wherein the first conductor comprises a first doped polycrystalline silicon layer and the second conductor comprises a second doped polycrystalline silicon layer.

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4. The device of claim 3, wherein the first doped polycrystalline silicon layer and the second doped polycrystalline silicon layer comprise n-type or p-type polycrystalline silicon.

5. The device of claim 2, wherein the substrate comprises doped silicon.

6. The device of claim 5, wherein the doped silicon substrate comprises n-type or p-type silicon.

7. The device of claim 1, wherein the gate is selected from the group consisting of: doped polycrystalline silicon, tungsten, tantalum, chromium, and aluminum.

8. The device of claim 1, further comprising a third insulating layer positioned between the gate and the first conductor and the second conductor.

9. The device of claim 1, wherein the distance from the first conductor to the second conductor through the tunneling barrier is about 10 nanometers.

10. The device of claim 1, wherein the at least one mobile charge comprises between 1 and about 100 ions.

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11. The device of claim 2, wherein the second insulating layer comprises silicon dioxide.

12. The device of claim 1, wherein the at least one mobile charge is at least one ion selected from the group consisting of: sodium, potassium, and lithium.

13. The device of claim 2, wherein the at least one mobile charge is introduced by diffusion.

14. The device of claim 13, wherein the at least one mobile charge is diffused into an insulating layer as the layer is formed.

15. The device of claim 1, wherein the at least one mobile charge is introduced by implantation.

16. The device of claim 1, wherein the first conductor, the second conductor, and the tunneling barrier comprise a single planarized surface.

17. The device of claim 16, wherein the single planarized surface is formed by Chemical Mechanical Planarization.

18. A current-controlling device comprising:

a substrate;

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an insulating layer on a surface of the substrate;

a first doped polycrystalline silicon layer and a second doped polycrystalline silicon layer on the insulating layer;

a tunneling barrier between the first doped polycrystalline silicon layer and the second doped polycrystalline silicon layer, the tunneling barrier comprising silicon dioxide;

at least one mobile charge positionable within the tunneling barrier;

wherein the first doped polycrystalline silicon layer, the second doped polycrystalline silicon layer, and the tunneling barrier comprise a single planarized surface formed by Chemical Mechanical Planarization;

a silicon dioxide layer on the single planarized surface; and

a gate formed on the silicon dioxide layer, wherein a voltage applied to the gate with respect to the substrate moves the at least one mobile charge to a position between the first conductor and the second conductor within the tunneling barrier, thus deforming the shape of the energy barrier between the first conductor and the second conductor;

whereby a current will flow between the first conductor and the second conductor when a voltage is present between the first conductor and the second conductor, the current flow resulting from quantum mechanical tunneling.

19. A method of forming a current-controlling device on a substrate, the method comprising:

forming a first insulating layer on the substrate;

creating a first conductor on the first insulating layer;

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shaping the first conductor to form a first tunneling contact area;

forming a second insulating layer on the surface of the first conductor;

creating a second conductor on the first and second insulating layers;

shaping the second conductor to form a second tunneling contact area;

planarizing the first conductor, the second insulating layer, and the second conductor to form a single planarized surface and a tunneling barrier between the first tunneling contact area and the second tunneling contact area, the tunneling barrier comprising the second insulating layer;

forming a third insulating layer on the single planarized surface;

introducing at least one mobile charge within at least one of the insulating layers, the mobile charge positionable within the tunneling barrier; and

creating a gate contact on the third insulating layer.

20. The method of claim 19, wherein the first insulating layer comprises silicon dioxide.

22. The method of claim 19, wherein all the insulating layers comprise silicon dioxide.

24. The method of claim 19, wherein the first conductor comprises n-type or p-type silicon.

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25. The method of claim 19, wherein the planarizing step comprises Chemical Mechanical Planarization.

26. The method of claim 19, further comprising implanting the at least one mobile charge in an insulating layer.

27. The method of claim 19, further comprising diffusing the at least one mobile charge in an insulating layer.

28. The method of claim 19, wherein the at least one mobile charge comprises between 1 and about 100 ions.

29. The method of claim 19, wherein the tunneling gap is about 10 nanometers wide.

30. A method of forming a current-controlling device on a substrate, the method comprising:

forming a first insulating layer on the substrate;

creating a first layer of doped polycrystalline silicon on the first insulating layer, the first layer of doped polycrystalline silicon comprising n-type or p-type silicon;

shaping the first layer of doped polycrystalline silicon to form a first tunneling contact area;

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forming a first silicon dioxide layer on the exposed surface of the first layer of doped polycrystalline silicon, the first silicon dioxide layer comprising between one and about 100 mobile ions;

creating a second layer of doped polycrystalline silicon on the first insulating layer and on the first silicon dioxide layer, the second layer of doped polycrystalline silicon comprising n-type or p-type silicon;

shaping the second layer of doped polycrystalline silicon to form a second tunneling contact area;

planarizing, by Chemical Mechanical Planarization, the first layer of doped polycrystalline silicon, the second insulating layer, and the second layer of doped polycrystalline silicon to form a tunneling gap between the first tunneling contact area and the second tunneling contact area, the gap comprising the first silicon dioxide layer and the mobile ions, the tunneling gap being between about 5 nanometers and about 15 nanometers wide;

forming a second silicon dioxide layer on the planarized surface; and

creating a gate contact layer on the third insulating layer.

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